PERGAMON

Engineering Fracture Mechanics 66 (2000) 387–402

Engineering Fracture Mechanics

www.elsevier.com/locate/engfracmech

Developing design rules to avert cracking and debonding in integrated circuit structures

X.H. Liu[a,*], Z. Suo[a], Q. Ma[b], H. Fujimoto[b]

[a]*Department of Mechanical and Aerospace Engineering and Princeton Materials Institute, Princeton University, Princeton, NJ 08544, USA*

[b]*Components Research, Intel Corporation, Santa Clara, CA 95052, USA*

Received 23 August 1999; received in revised form 19 January 2000; accepted 26 January 2000

Abstract

In an integrated circuit, stresses come from many sources (e.g., differential thermal expansion and electromigration). The circuit structures are never perfect, possibly containing crack-like flaws. The stresses may drive the pre-existing cracks to grow and cause circuit failure. We explore a fracture mechanics approach to formulate design rules to avert crack growth. We adopt a strategy based on two attributes of integrated circuits. First, high tensile sress is generated by internal misfit, and is therefore confined in small regions with size comparable to the feature dimension. Second, the fabrication process is controlled down to the individual features, so that the pre-existing cracks are expected to be smaller than the feature sizes. Instead of considering pre-existing crack, we consider all possible pre-existing cracks, and require that none of them should grow. Such a no-cracking condition is independent of the nature of pre-existing cracks; rather, it depends on parameters that define a circuit structure, such as the feature size and the aspect ratios of the geometry. Furthermore, the stress singularity at sharp corners in a circuit structure does not cause any particular difficulty. We illustrate these ideas with elementary examples involving blanket films and isolated interconnect lines. Then in the spirit of design rules, we investigate a multilevel interconnect test structure to avert channeling cracks caused by differential thermal expansion.

Keywords: Integrated circuits; Design rules; Residual stresses; Energy release rate; Finite element method

* Corresponding author. IBM T.J. Watson Research Center, P.O. Box 218, Yorktown Heights, NY 10598, USA. Tel.: +1-914-945-2313; fax: +1-914-945-4506.

E-mail address: xhliu@us.ibm.com (X.H. Liu).

0013-7944/00/$ - see front matter
PII: S0013-7944(00)00024-2

1. Introduction

Electrical functions aside, an integrated circuit is a heterogeneous material structure of small feature sizes. Structural failures, such as cracking and debonding, may arise during fabrication and operation. As the circuit geometry becomes more complex, with new materials and processes constantly being introduced, it is imperative to develop design rules to avert structural failures. Fig. 1 shows a multi-level interconnect structure on a silicon chip. Embedded in a silicon dioxide matrix are aluminum lines in several levels which are connected by tungsten studs. The metal network transports electrical currents among the transistors in the chip. Major sources of stresses are listed below.

- The material deposition process can generate stress, known as intrinsic stress. For example, a chemical vapor deposited tungsten blanket film has a tensile stress on the order of 1 GPa [1,2].
- Dissimilar materials are integrated on a chip. When the structure is cooled from the processing temperature, differential thermal contraction leads to stresses [3,4].
- When a circuit is in use, the electric current can cause mass diffusion (i.e., electro-migration) in aluminum lines. Voids form where mass depletes, and pressure arises where mass accumulates [5–7].
- During packaging, when a chip is bonded to a polymer or a ceramic substrate, additional thermal stress is generated [8].

In the recent decade, the microelectronic industry has developed several basic capabilities dealing with

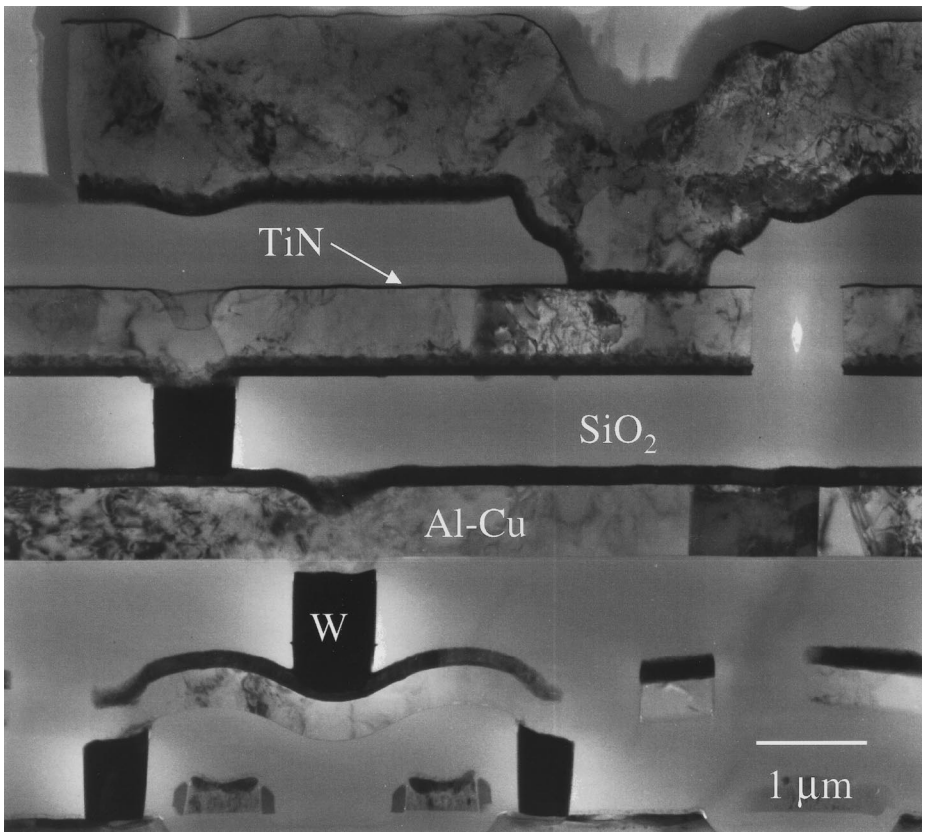


Fig. 1. TEM cross-section of a typical multilayer interconnect structure (Courtesy of John Mardinly, Intel Corporation.)

the problem of stress. Stresses in simple structures, e.g., blanket films and parallel lines on a substrate, can be measured with wafer curvatures and X-ray diffraction [1,3]. The measurements provide material data, such as yield strength and intrinsic stress. Based on the data, one can develop finite element models to calculate stress fields in more complex structures [1–4]. Good correlations have been found between the measured and the calculated average stresses. It is unclear, however, how the stresses can be used to predict cracking or debonding. No design rules have been established to avoid structural failures of integrated circuits.

Fig. 2 illustrates two well-known design approaches for bulk structures: one based on stress, and the other on energy. In the stress approach, one measures the fracture strength S of a material using a simple specimen (e.g., a bar under uniaxial tension). One then calculates the stress field in a real structure and finds the maximum stress in the structure, $\sigma_{\max}$. If the maximum stress is below the strength, $\sigma_{\max} < S$, the structure is considered to be safe. Two basic difficulties arise when the approach is applied to integrated circuits. First, the fracture strength of a material is an ill-defined quantity; the strength measured from a free-standing sample has little to do with the same material integrated in a structure with a small feature size. Second, the stress field in an integrated circuit is sensitive to geometric details, and possibly singular at corners.

In the energy approach, one measures the fracture energy Γ of a material using a specimen with an intentionally introduced crack. One then calculates the energy release rate $\mathcal{G}$ of a pre-existing crack in a real structure. If the energy release rate is below the fracture energy, $\mathcal{G} < \Gamma$, the crack in the structure will not grow. For example, for a pre-existing crack of length $2a$ in an infinite elastic solid subject to a tensile stress σ (Fig. 2(b)), the crack cannot grow if $\pi\sigma^2 a/E < \Gamma$, where E is Young's modulus. The fracture mechanics approach requires the information of the pre-existing crack (i.e., its location, orientation, and size). Such information, however, is impossible to obtain for integrated circuit structures. Consequently, a main issue in applying fracture mechanics to integrated circuits is how to treat pre-existing cracks. This issue is the focus of this paper.

In Section 2, by reviewing results for simple geometries involving blanket films or isolated lines [9–20], we will show that the design rules to avoid cracking and debonding in complex integrated circuits can

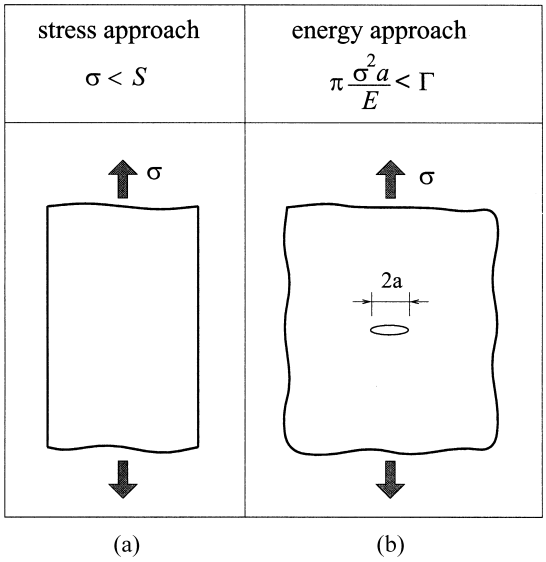


Fig. 2. Two well-known design approaches for bulk structures.

be put into a general formula that is independent of crack length and involves only material and geometry parameters. This is obtained by considering all the possible pre-existing cracks and requiring that the largest possible energy release rate is less than the corresponding fracture energy. In Section 3, we will study a multi-layer interconnect structure in the spirit of design rules.

2. No-cracking condition

When the fracture mechanics is applied to a bulk structure, an essential input is information about a pre-existing crack, i.e., its location, size, and orientation. This information is impossible to obtain in practice for an integrated circuit. Two basic attributes of integrated circuits, however, suggest a different approach. First, high tensile stress is generated by internal misfit, and is therefore confined in small regions of size comparable to the feature dimension. Second, the fabrication process is controlled down to the individual features, so that the pre-existing cracks are expected to be smaller than the feature sizes. Instead of considering one pre-existing crack, we consider all possible pre-existing cracks, and require that none of them should grow. Such a no-cracking condition needs no information on pre-existing cracks; rather, it depends on parameters that define a circuit structure, such as the feature size and the aspect ratios of the geometry. The approach has been developed to analyze cracking induced by thermal expansion misfit in structures containing small objects, such as inclusions, grains, fibers, and thin films [9–16]. In this paper, we apply this approach to integrated circuit structures.

The design rules to avoid cracking and debonding take the following general form:

$$\beta\frac{\sigma^2 h}{M} < \Gamma \tag{1}$$

where, σ is a stress level representative of a given source, and M is a suitable elastic modulus. The length h is the feature size of the structure (e.g., film thickness or interconnect line width). The dimensionless parameter β depends on ratios of parameters characterizing the structure, such as elastic moduli and various lengths. In application to integrated circuit structures, one needs to determine the values of the variables at the left-hand side of Eq. (1) by calculating the energy release rate for all the possible pre-existing cracks, while the corresponding fracture energy, Γ, can be measured experimentally. Although the details have been published in literature, the simple examples which follow are used to illustrate the origin of the no-cracking condition. For the time being, we consider elastic systems, so that the fracture energy Γ directly relates to surface and interface energy densities.

2.1. Thin film on substrate

First consider a thin film grown on a thick substrate. At the deposition temperature T_0, the film acquires a biaxial intrinsic stress σ_0. Upon cooling to temperature T, an additional biaxial stress is generated due to differential thermal contraction. The total residual stress is

$$\sigma = \sigma_0 + \frac{E_f}{1-\nu_f}(\alpha_f - \alpha_s)(T_0 - T), \tag{2}$$

where α_f and α_s are the thermal expansion coefficients of the film and the substrate, and E_f and ν_f are Young's modulus and Poisson's ratio of the film. The intrinsic stress may depend on the film thickness; for simplicity, such dependence is neglected in the following discussion. Thus, the total residual stress in the film is independent of the film thickness.

The residual stress may cause various forms of failures. Fig. 3(a) shows a film debonding from an

edge. As the debond length increases, the energy release rate also increases (Fig. 3(d)). When the debond length is several times the film thickness, the energy release rate approaches a steady value, which equals the stored elastic energy per unit area of the bonded film:

$$\mathcal{G}_s = \frac{1-\nu_f}{E_f}\sigma^2 h \tag{3}$$

where, h is the film thickness, and σ the residual stress given by Eq. (2). Let Γ be the film/substrate interface fracture energy. If $\mathcal{G}_s < \Gamma$, an initial defect of *any* size will not grow on the interface. The condition $\mathcal{G}_s < \Gamma$ can be put into the form of Eq. (1) by taking $\beta = 1$ and $M = E_f/(1-\nu_f)$. In using Eq. (1), one needs no information of initial flaws.

Next consider a crack channeling in the film (Fig. 3(b)). The energy release rate as a function of the crack length follows the same trend as in Fig. 3(d). Condition (1) still holds, but with a different β, depending on the ratios of elastic constants [17]. Also, Γ should be the fracture energy of the film material, namely, for a purely elastic system, $\Gamma = 2\gamma_s$. For a circular blister of a film under biaxial compression (Fig. 3(c)), $\beta = 1$ at large blister radius [18], and Γ is the interface fracture energy. In all the three cases in Fig. 3, energy release rate has an upper limit. These forms of failure are avoided if the conditions like Eq. (1) are all satisfied.

Experience indicates that, everything else being equal, a thick film is more likely to crack or debond than a thin film. The phenomenon is understood in terms of Eq. (1). As the film becomes thinner, the amount of the stored elastic energy per unit area of the film decreases, but the fracture energy remains the same. Consequently, when the film thickness is below a critical value, the elastic energy is insufficient to cause cracking or debonding.

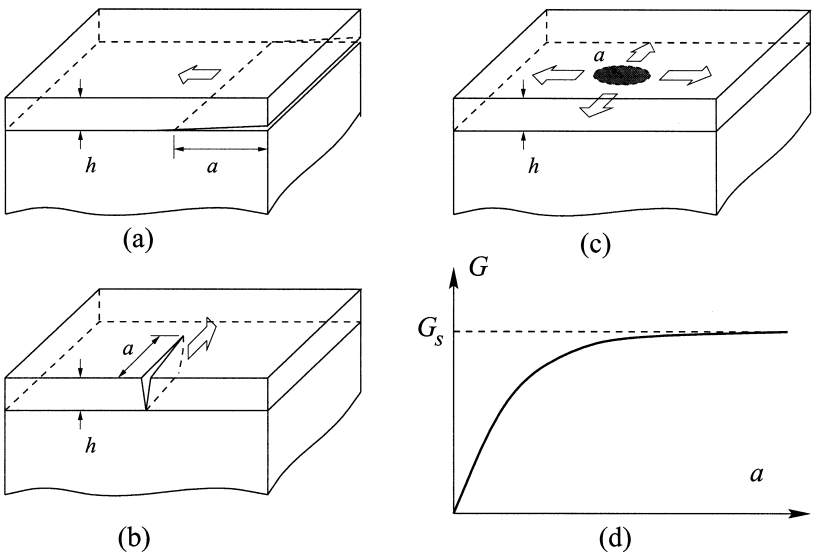


Fig. 3. (a) Debond at film and substrate interface. (b) Channeling crack in a film bonded to a substrate. (c) Blister debond at film and substrate interface when the film is subject to biaxial compression. (b) The trend of the energy release rate $\mathcal{G}$ as a function of crack length a.

2.2. Interconnect line in insulator matrix

In some structures, the energy release rate as a function of crack size, has a maximum. Fig. 4 shows an aluminum line in an oxide matrix. The line is under pressure due to electromigration [7]. As a result, the matrix is subjected to a tensile hoop stress. For simplicity, first consider a line of a circular cross-section (Fig. 4(a)). The stress in the matrix is non-uniform, high near the cylinder and vanishing far away from the cylinder. Whether the hoop stress will cause cracking depends on flaw characteristics: where and how large the flaw is. Such information is usually unavailable. Consequently, whether or not the matrix will crack is a statistical prediction. One can, however, set a deterministic design rule on the basis of the worst scenario.

Consider flaws of *all* sizes in the matrix. Fig. 4(c) sketches the energy release rate, $\mathscr{G}$, as a function of the flaw size, a. The energy release rate is small for very small flaws. For very large flaws, because the stress in the matrix decays far away from the cylinder, the energy release rate is also small. Consequently, the energy release rate reaches maximum, $\mathscr{G}_{\max}$, for a flaw of an intermediate size. For a cylinder of radius R under compressive stress σ, the maximum occurs at $a = R/2$ and $\mathscr{G}_{\max} = 0.058(1 - \nu^2)\sigma^2 R/E$ [13], where E is Young's modulus and ν Poisson's ratio. If this maximum energy release rate is below the fracture energy of the matrix material, $\mathscr{G}_{\max} < \Gamma$, no flaw can grow. Thus, condition (1) holds, where $\beta = 0.058$, and h and M are replaced by R and $E/(1 - \nu^2)$, respectively. Once again, the no-cracking condition depends only on well-defined geometric and material parameters, but not on any

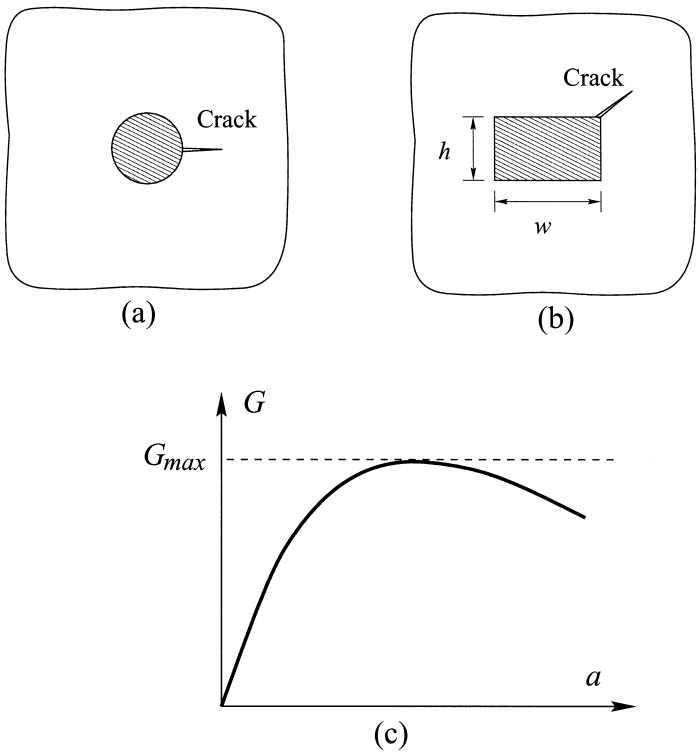


Fig. 4. A brittle insular matrix containing an interconnect line under pressure. (a) An interconnect line of circular cross-section. (b) A line with rectangular cross-section. (c) $\mathscr{G}$ vs. a curve.

information regarding pre-existing cracks. Everything else being equal, a cylinder of a large radius is more likely to cause the matrix to crack than that of a small radius.

In the above case, we have assumed that the elastic constants of the matrix and the cylinder are similar. The effect of dissimilar elastic moduli has been treated in Ref. [15]. For a line with a rectangular cross-section (Fig. 4(b)), the stress field in the matrix is singular near the corners of the line. The energy release rate cannot be found in a simple analytical form, but still follows the trend of Fig. 4(c). In this case, β is a function of the aspect ratio w/h. Note that the presence of corner singularity causes no difficulty in our consideration.

2.3. Thin film on substrate, another situation

In Section 2.1 and Fig. 3(b), we have considered an initial flaw in the film spreading in the direction parallel to the interface. Another situation, often more relevant in practice, is an initial flaw running across the film in the thickness direction, penetrating the interface, and dipping into the substrate. For example, when the film is a diffusion barrier or an electrical insulator, a crack locally penetrating the film, without lateral spreading, is enough to cause circuit malfunction. To simplify the discussion of such through-thickness crack growth, we idealize the initial flaw as a full channel of depth a, which is smaller than the film thickness (Fig. 5(a)). We examine whether the flaw will propagate in the thickness direction into the substrate (Fig. 5(b)). The qualitative conclusion, however, is applicable to a thumb-shaped initial flaw. We distinguish two cases according to the relative elastic modulus of the film and the substrate.

For a compliant film on a stiff substrate, the energy release rate vanishes when the crack tip hits the film-substrate interface, $a = h$. The energy release rate also vanishes when the crack is either much smaller or much larger than the film thickness. Consequently, the energy release rate attains one

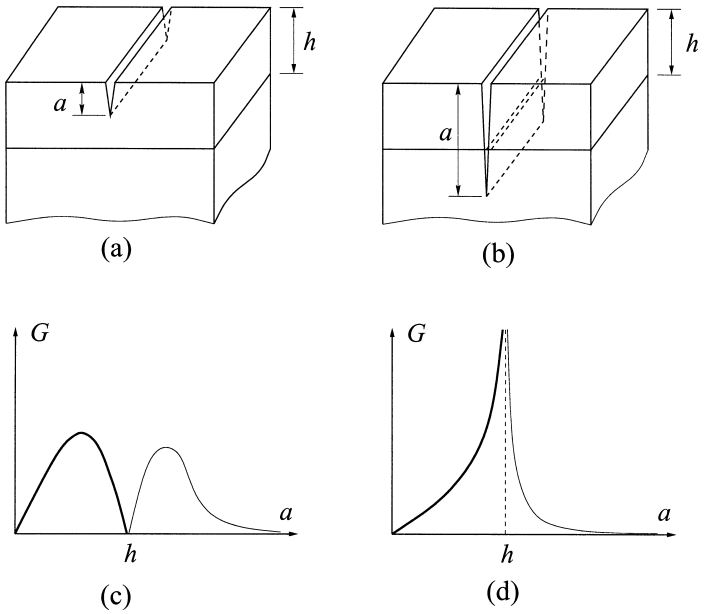


Fig. 5. (a) Initial flaw in the film. (b) Crack running in the thickness direction. (c) $\mathscr{G}$ versus a curve for compliant film on stiff substrate. (d) $\mathscr{G}$ vs. a curve for stiff film on compliant substrate.

maximum when the crack tip is in the film, and another maximum when the crack tip is in the substrate (Fig 5(c)). When the maximum in the film is below the fracture energy of the film, any flaw in the film cannot grow, leading to the no-cracking condition (1). The situation is similar to that discussed in Section 2.2.

For a stiff film on a compliant substrate, the energy release rate is unbounded when the crack approaches the film-substrate interface. Once the crack penetrates the substrate, the energy release rate decreases sharply as the crack length increases (Fig. 5(d)). In this case, it is too stringent to require that flaws of all sizes do not grow. When a film is well prepared, all initial flaws in the film must be small compared to the film thickness, say, $a < h/2$. We require that the maximum flaw does not grow. Consequently, the no-cracking condition (1) still holds. The boundary value problems have been analyzed in Ref. [19] from which the β-values can be extracted. The size dependance here is similar to the known problem of a free-standing glass fiber. A glass fiber is usually stronger than a large-radius glass cylinder simply because the flaws in the fiber are necessarily small, and those in the cylinder are possibly large.

It is instructive to compare the above examples with the Griffith problem (Fig. 2(b)): a crack of size $2a$ in an infinite body subject to remote tension σ. In the Griffith problem, the energy release rate increases linearly with the crack size, and the initial flaw size can be of any size in the bulk structure. For an integrated circuit, however, the energy release rate often has a steady value or a maximum, and the initial flaw size is expected to be smaller than the circuit feature size. In any event, the largest possible energy release rate scales with the feature size. Consequently, we can obtain the no-cracking condition based on the feature size, rather than the initial flaw size. This greatly facilitates the application of fracture mechanics in integrated circuit structures.

3. A multi-layer inteconnect test structure

In this section, we examine a test structure for establishing design rules to avert cracking in

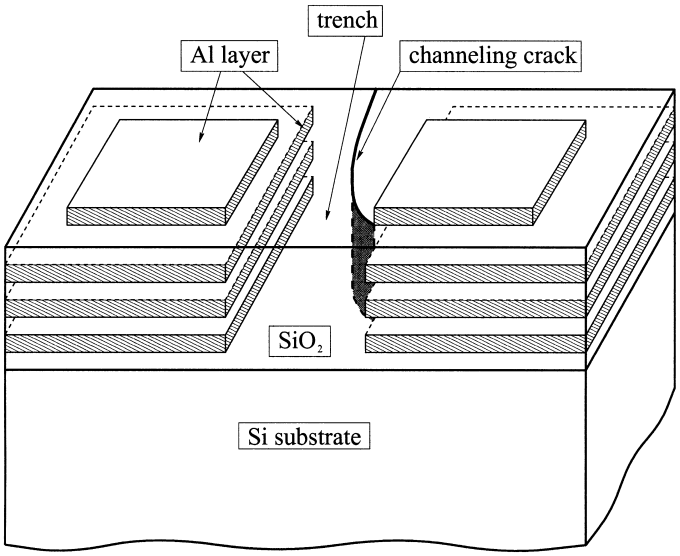


Fig. 6. A multi-level interconnect structure with a crack.

interconnect circuits. Fig. 6 illustrates the structure of multi-layer interconnects, consisting of a silicon substrate and a silicon dioxide film, within which two stacks of aluminum pads are embedded. On the oxide film surface, there are two additional aluminum pads. It was observed that a crack, initiated at the corner of a pad, propagated in the oxide trench between the two stacks; see also Fig. 7. The reason for cracking in this structure is two folds. First, as aluminum has a larger thermal expansion coefficient than silicon and silicon dioxide, upon cooling, thermal expansion misfit induces a tensile stress in the trench. Second, the volume of the oxide trench is large, so that such a crack can release a large amount of elastic energy.

Fig. 8 illustrates the cross-section of the structure. Instead of exploring all structural designs, we limit our attention as follows. Three layers of aluminum pads lie inside the oxide. All the pads have the same thickness h_1 including the surface pads, and they are equally spaced in the oxide with the spacing h_2. The oxide trench depth is $H = 3h_1 + 4h_2$ and the trench width w is fixed to be $w/H = 2/7$. The thickness and width of the silicon substrate are about $400H$. The thermomechanical properties are fixed in calculations (Table 1). The generalized plane strain conditions are assumed. The commercial code, ABAQUS, is used to compute the displacement and stress fields.

Far away from the oxide trench, the stress state in all the aluminum pads is uniform and biaxial. This stress is identical to that in a single blanket aluminum film bonded on a silicon substrate. Before the blanket film undergoes plastic deformation, the biaxial stress is linear in the temperature drop ΔT:

$$\sigma_{\mathrm{bf}} = \frac{E_{\mathrm{Al}}}{1 - \nu_{\mathrm{Al}}}(\alpha_{\mathrm{Al}} - \alpha_{\mathrm{Si}})\Delta T. \tag{4}$$

A similar expression gives the stress in the oxide far away from the trench. Here we ignore any intrinsic stress. Because $\alpha_{\mathrm{Al}} > \alpha_{\mathrm{Si}} > \alpha_{\mathrm{SiO_2}}$, far away from the trench, the aluminum pad is in tension and the oxide layer is in compression.

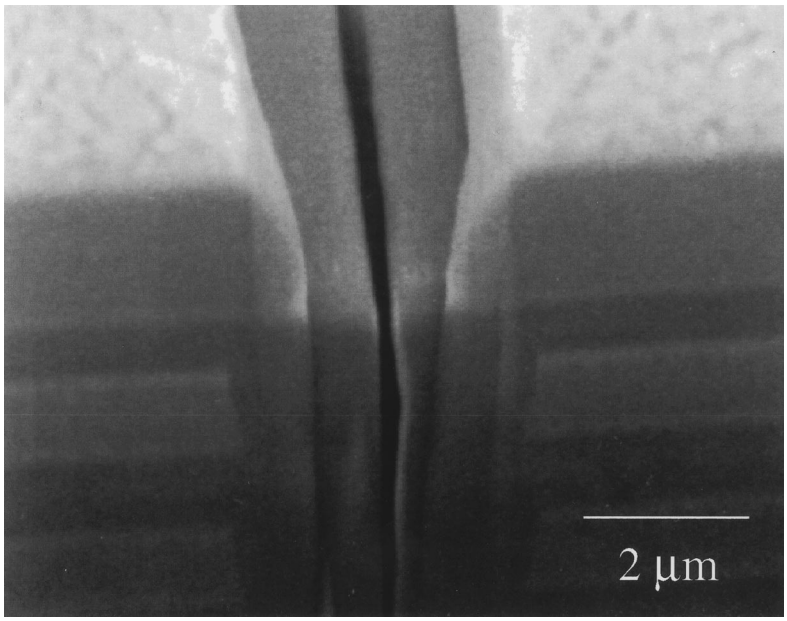


Fig. 7. A channeling crack in a trench between metal pads. At the up-left and the up-right are two surface pads. One can see two layers of metals, respectively, at the down-left and the down-right. The channeling crack lies in the middle.

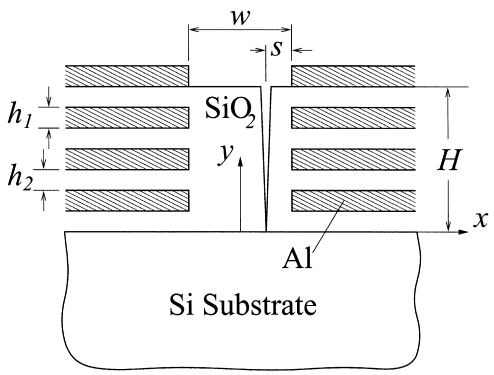


Fig. 8. Cross-section view of the multi-level interconnect structure.

When the aluminum pads undergo plastic yielding, the stress is no longer given by Eq. (4). In our calculations, aluminum is idealized as elastic-perfectly plastic material with a constant yield strength σ_0. A blanket alumium film yields at a temperature drop ΔT_0, given by

$$\Delta T_0 = \frac{1-\nu_{\mathrm{Al}}}{E_{\mathrm{Al}}}\frac{\sigma_0}{\alpha_{\mathrm{Al}}-\alpha_{\mathrm{Si}}}. \tag{5}$$

When the temperature decreases further, the biaxial stress remains at the yield strength σ_0, while the stress in the oxide keeps increasing linearly with ΔT.

The stress field close to the oxide trench cannot be found in closed form; neither can the energy release rate for a channeling crack in the trench. These are obtained from finite element analysis. First consider the stress field in the structure without the crack. Fig. 9(a) shows a typical finite element mesh, consisting of 25,273 nodes and 24,360 bilinear quadri-lateral elements. Around the trench, the mesh is refined to resolve the stress concentration (Fig. 9(b)). The elastic–plastic boundary value problem is solved incrementally by decreasing the temperature step by step.

Fig. 10 shows the stress component σ_x at $y/H = 0.5$, a horizontal line that runs in the second level aluminum pads and the oxide trench. As the temperature drops, the stress in aluminum far away from the trench is set at the yield stress. Close to the oxide trench, the stress increases with the temperature drop. It attains $2.5\sigma_0$ at $\Delta T/\Delta T_0 = 8$. The stress in aluminum can exceed the yield stress because of the triaxial stress state resulting from the oxide constraint. The stress σ_x at $y/H = 0.643$ is shown in Fig. 11. Note that away from the trench, the magnitude of the stress in the oxide layer increases linearly with the temperature drop ΔT.

When channeling crack occurs at the location s (Fig. 8), the stresses in the area comparable to the trench width times the trench depth are partially released. In the finite element model, we approximated this stress relief process by an elastic unloading. On the crack surfaces we applied $-\sigma(y)$, which was

Table 1
Material constants used for silicon, silicon dioxide and aluminum alloy

Material	E (GPa)	ν	α (10^{-6} K^{-1})	σ_0 (MPa)
Si	150	0.28	3.0	–
SiO_2	75	0.25	1.0	–
Al	71	0.35	23.6	100

calculated at the location s prior to the introduction of the crack. The crack opening displacement, $\delta(y)$, was obtained by the finite element analysis. The elastic energy release due to the introduction of the crack is then [15],

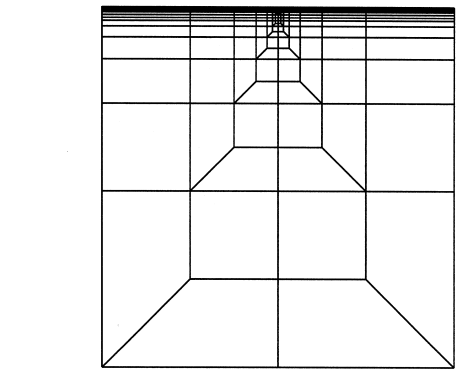
$$\mathscr{G} = \frac{1}{2H}\int_0^H \sigma(y)\delta(y)\,\mathrm{d}y. \tag{6}$$

We write

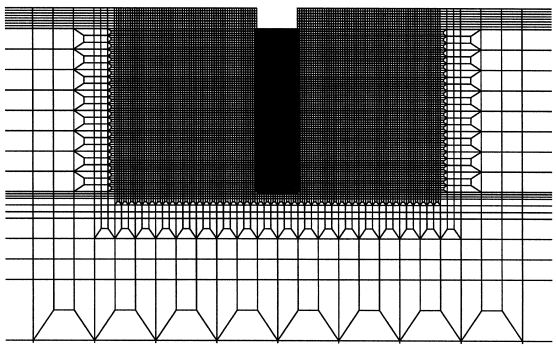
$$\mathscr{G} = \beta\frac{\sigma_0^2 H}{E_{\mathrm{Al}}}. \tag{7}$$

The non-dimensional quantity β was obtained from the finite element analysis. The calculations were repeated for various length ratios, s/W and h_1/h_2. The design rules can be put into form (1), where h is replaced by H, M by E_{Al}, and σ by σ_0. Here, Γ is the fracture energy of silicon dioxide.

Fig. 12 shows the dimensionless energy release rate, i.e., β in Eq. (7), as a function of temperature change. Also included for comparison is the result, assuming that aluminum remains



(a)



(b)

Fig. 9. (a) Typical finite element mesh. (b) Refined mesh around the trench.

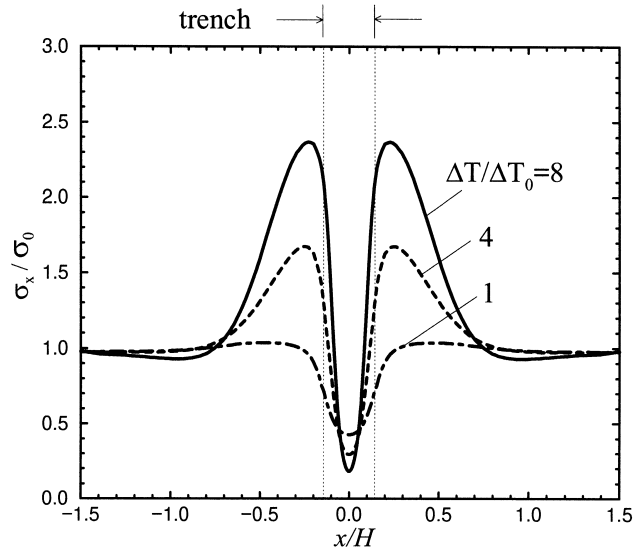


Fig. 10. Stress σ_x at $y/H = 0.5$.

purely elastic, which follows a parabolic curve since the energy release rate is proportional to $(\Delta T)^2$. After aluminum yielding, the energy release rate is significantly smaller than the elastic case.

The effect of aluminum pad thickness is presented in Fig. 13. The energy release rate strongly depends on the pad thickness. For a fixed trench depth H, decreasing aluminum fraction h_1/h_2 reduces the cracking driving force.

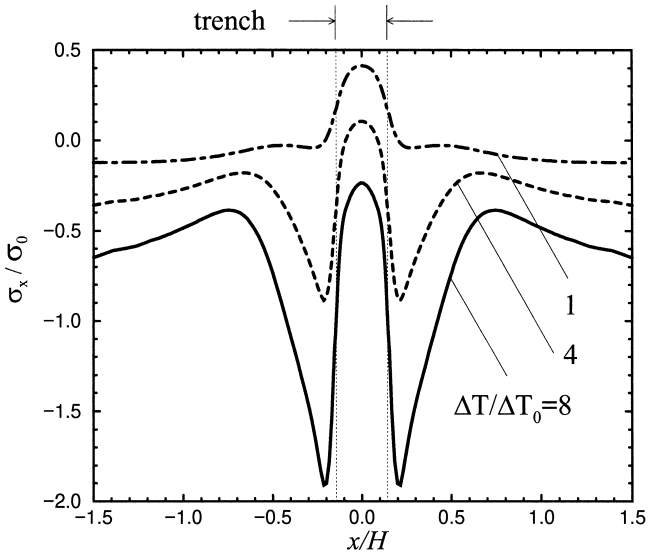


Fig. 11. Stress σ_x at $y/H = 0.643$.

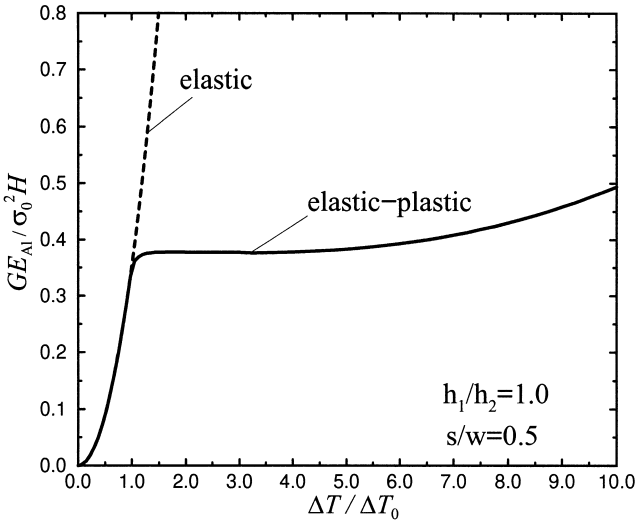


Fig. 12. Non-dimensional energy release rate as a function of temperature change.

Fig. 14 shows the energy release rates for various crack positions s/W. The energy release rates are nearly the same for all crack positions before aluminum yields, consistent with the findings in Ref. [20]. However, after aluminum yields, energy release rates vary with the crack position appreciably. The crack closer to the wall ($s/w = 0.03$) has larger energy release rate. This is due to the high constraint by the large triaxial stress in the embedded aluminum near the edges. A crack path close to the wall can greatly release elastic energy. The actual crack position, however, cannot be obtained from the previous analysis. It should be determined by the criterion that a crack in a brittle material follows a path of

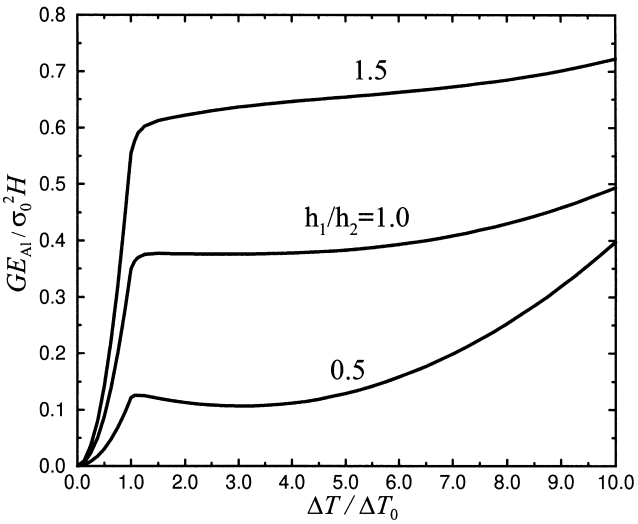


Fig. 13. Energy release rate for various pad thickness ratios.

pure mode I. For our structure, the pure mode I path is located in the center and this path was indeed observed in experiments (Fig. 7).

4. Concluding remarks

The application of fracture mechanics normally requires information of pre-existing cracks in structures. Yet, in practice, it is impossible to obtain such information for integrated circuits — the heterogeneous material structures with small feature sizes. This paper outlines a framework to develop design rules to avert cracking by using information of the circuit structures, rather than that of pre-existing cracks. Two basic attributes of integrated circuits make such design rules possible. First, in many situations, the stress field is induced by some internal misfit, so that high tensile stress is confined in regions of size comparable to the feature dimension. Second, the pre-existing cracks are expected to be smaller than the feature size. Consider all possible cracks in a structure and require the energy release rate of every crack to be below a suitable fracture energy. If there is a maximum among the energy release rates of all cracks, we require this maximum to be below the fracture energy. If the energy release rate as a function of the crack size is unbounded, we assume that all pre-existing cracks are of sizes smaller than some fraction of the feature size, and require the largest energy release rate to be below the fracture energy. In either case, our design rule takes the form of Eq. (1). To further develop this approach, finite element calculations for critical structures are needed. This paper focuses on issues concerning initial flaws. In our discussion on design rules in Section 2, we used only linear elastic fracture mechanics to calculate energy release rate. Nevertheless, the design rules can be extended to integrated circuit structures with plasticity effects, as in the test structures presented in Section 3 where plasticity effect was included to compute energy release rate. However, no attempt has been made in this

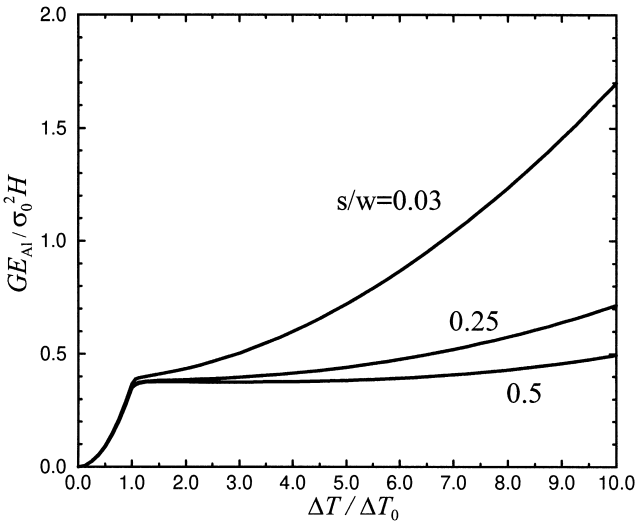


Fig. 14. Energy release rate for various crack locations.

paper to address the complications involving the fracture energy [21–23]. It is understood that fracture energy is affected by inelastic dissipation. Furthermore, a material exposed to a moisture environment may have a much lower fracture energy [24,25]. A conservative design rule may use the threshold value of the fracture energy. These issues await further investigations.

Acknowledgements

The work is supported by a grant to Princeton University from Intel Corporation. XHL and ZS are partly supported by the Institute for Materials Research and Engineering, Singapore, and by DARPA (N6001-98-1-8916). These supports are gratefully acknowledged.

References

[1] Lee J, Ma Q, Marieb T, Mack AS, Fujimoto H, Flinn P, Woolery B, Keys L. Measurement and modeling of intrinsic stresses in CVD W lines. Mater Res Soc Symp Proc 1995;391:115–9.
[2] Ma Q, Lee J. Fujimoto H. Probing stresses in metal trenches using Raman piezospectroscopy. Advances in Electronic Packaging, EEP 1997;19(1):1233–8.
[3] Greenebaum B, Sauter AI, Flinn PA, Nix WD. Stress in metal lines under passivation; comparison of experiment with finite element calculations. Appl Phys Lett 1991;58:1845–7.
[4] Shen YL, Suresh S, Blech IA. Stresses, curvatures, and shape changes arising from patterned lines on silicon wafers. J Appl Phys 1996;80:1388–98.
[5] Blech IA. Electromigration in thin aluminum films on titanium nitride. J Appl Phys 1976;47:1203–8.
[6] Korhonen MA, Borgesen P, Tu KN, Li CY. Stress evolution due to electromigration in confined metal lines. J Appl Phys 1993;73:3790–9.
[7] Suo Z. Stable state of interconnect under temperature change and electric current. Acta Mater 1998;46:3725–32.
[8] Liu XH, Suo Z, Ma Q. Split singularities: stress field near the edge of silicon die on polymer substrate. Acta Mater 1999;47:67–76.
[9] Lange FF. Fracture criteria for crack extension and arrest in residual, localized stress fields associated with second phase particles. Fracture Mechanics of Ceramics 1976;2:599–609.
[10] Evans AG. Microfracture from thermal expansion anisotropy. Part I: single phase system. Acta Metall 1978;26:1845–53.
[11] Clarke DR. Microfracture in brittle solids resulting from anisotropic shape change. Acta Metall 1980;28:913–23.
[12] Tvergaard V, Hutchinson JW. Microcracking in ceramics induced by thermal expansion or elastic anisotropy. J Am Ceram Soc 1988;71:157–66.
[13] Lu TC, Yang J, Suo Z, Evans AG, Hecht R. Mehrabian R. Matrix cracking in intermetallic composites caused by thermal expansion mismatch. Acta Metall Mater 1991;39:1883–90.
[14] Hutchinson JW, Suo Z. Mixed mode cracking in layered materials. Advances in Applied Mechanics 1991;29:64–191.
[15] Ho S, Suo Z. Microcracks tunneling in brittle matrix composites driven by thermal expansion mismatch. Acta Metall Mater 1992;40:1685–90.
[16] Evans AG, Hutchinson JW. Thermomechanical integrity of thin films and multilayers. Acta Mater 1995;43:2507–30.
[17] Beuth JL. Cracking of thin bonded films in residual tension. Int J Solids Structures 1992;29:1657–75.
[18] Evans AG, Hutchinson JW. On the mechanics of delamination and spalling in compressed films. Int J Solids Structures 1984;20:455–66.
[19] Ye T, Suo Z, Evans AG. Thin film cracking and the roles of substrate and interface. Int J Solids Structures 1992;29:2639–48.
[20] Liu XH, Suo Z, Ma Q, Fujimoto H. Cracking and debonding in integrated microstructures. Mater Res Soc Symp Proc 1998;516:313–24.
[21] Bagchi A, Lucas GE, Suo Z, Evans AG. A new procedure for measuring the decohesion energy for thin ductile films on substrates. J Mater Res 1994;9:1734–41.
[22] Ma Q, Bumgarner J, Fujimoto H, Lane M, Dauskardt RH. Adhesion measurement of interfaces in multilayer interconnect structures. Mater Res Soc Symp Proc 1997;473:3–14.
[23] Ma Q, Xie J, Chao S, El-Mansy S, McFadden R, Fujimoto H. Channeling cracking technique for toughness measurement of brittle dielectric thin films on silicon substrates. Mater Res Soc Symp Proc 1998;516:331–6.

[24] Ma Q, Tran Q, Pan C, Fujimoto H, Chiang C. Polymer/metal interfaces in interconnect structures: moisture diffusion and stress corrosion effects. Mater Res Soc Symp Proc 1998;511:329–39.
[25] Dauskardt RH, Lane M, Ma Q, Krishna N. Adhesion and debonding of multilayer thin film structures. Eng Fract Mech 1998;61:141–62.