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The effect of stress on the dielectric properties of barium strontium titanate thin films

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Barium strontium titanate thin films are being developed as capacitors in dynamic random access memories. These films, grown on silicon substrates, are under tensile residual stress. By a converse electrostrictive effect, the in-plane tensile stress reduces the capacitance in the thickness direction of the film. We measured the substrate curvature change upon the removal of the film, and found the magnitude of the residual stress to be 610 MPa. In a separate experiment, we applied a force to vary the stress in a film on a substrate, and simultaneously recorded the capacitance change of the film. The measurements quantify the effect of stress on thin film capacitance. The stress free capacitance was found to be 23% higher than the capacitance under residual stress. [S0003-6951(99)02340-2]

Due to their large permittivities, barium strontium titanate (BST) bulk ceramics have long been used to make high charge-density capacitors. Thin films of BST are now being developed to replace silica–nitride laminates in dynamic random access memories. The capacitance of the BST films, however, is much lower than that anticipated from the bulk BST permittivity. Figure 1 compares the temperature-dependent dielectric constant of a bulk ceramic $Ba_{0.7}Sr_{0.3}TiO_3$ to that of a film of the same composition. The bulk ceramic undergoes the paraelectric-to-ferroelectric phase transition near room temperature, where the dielectric constant peaks. For the film, the dielectric constant is much lower, and has no sharp peak.

Possible causes for the permittivity reduction in the film include fine grains, interfacial capacitance, and residual stress. The permittivity of bulk ferroelectric ceramics has long been known to vary with grain size. A recent model suggests that a bulk ceramic consists of high permittivity grains and low permittivity grain boundaries, in series.[1] The smaller the grain size, the smaller the grain-to-boundary ratio, and the smaller the overall permittivity of the ceramic. This mechanism is less important in thin films where grains are columnar, with all the grain boundaries and the grains in parallel.[2] The effect of fine grains on the permittivity of the BST films remains unclear.[3]

A second possible cause for the permittivity reduction is interfacial capacitance. Experimental data of the capacitance as a function of the film thickness fit an empirical relation:[4–6]

$$\frac{1}{c}=\frac{1}{c_i}+\frac{t}{\varepsilon_f}. \tag{1}$$

Here c is the capacitance per unit film area, and t the film thickness; c_i and ε_f are fitting parameters. This relation can be interpreted as follows.[7] In a film, near either film–electrode interface the ionic contribution to the dielectric response is suppressed—that is, a region a few lattice constant thick acts as a low permittivity or ''dead'' layer. An applied voltage is dropped across the interfacial layers and the bulk of the film in series. Consequently, c_i and ε_f are interpreted, respectively, as the interfacial capacitance and the film permittivity. The effect of c_i is more pronounced for thinner films.

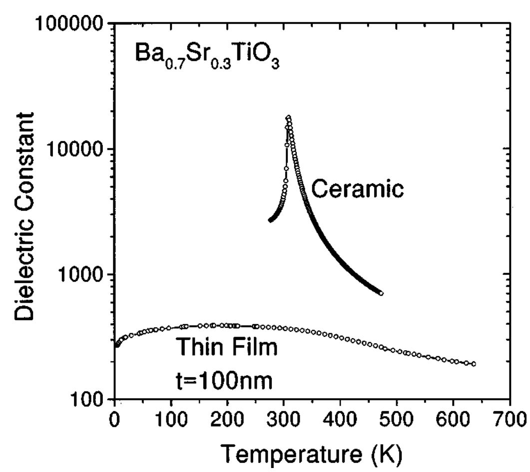

FIG. 1. Variation of the dielectric constant of a bulk ceramic and a film as a function of temperature.

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A third cause for the permittivity reduction is the residual stress in the film. For a free-standing film, a voltage applied across its thickness causes the film to contract in its plane by an electrostrictive strain $Q_{12}D^2$. Here Q_{12} (<0) is the electrostrictive coefficient, and D the electric displacement. A BST film on a silicon substrate, however, is under a tensile residual stress, σ. For a thin film in the paraelectric phase the thermodynamic theory of Devonshire predicts a converse electrostrictive effect.[8] The stress in the plane of the film causes a change in the permittivity measured through the film thickness:

$$\frac{1}{\varepsilon_f}=\frac{1}{\varepsilon_u}-4Q_{12}\sigma, \tag{2}$$

where ε_f is the permittivity of the stressed film, and ε_u the permittivity of the unstressed film. Because $Q_{12}<0$, a residual tensile stress in the film reduces the permittivity. This formula is valid for all dielectrics. For a high-permittivity film grown on a substrate, because ε_u and σ are large, the change in permittivity due to stress can be pronounced. This formula is valid provided the film remains in the paraelectric phase.

Pertsev *et al.* recently has proposed that substrate constraint can affect the ferroelectric phase transitions in thin films.[9,10] The tensile misfit strain in the film is suggested to induce in barium titanate films a transition to a ferroelectric phase in which the polarization axis lies in the plane of the film. At the transition a deviation from the Curie–Weiss law is predicted. The model provides a good description of the temperature dependence of the capacitance of the dielectric constant of BST films.[11] The films studied in this letter show Curie–Weiss behavior above about 350 K but at room temperature exhibit a significant deviation form the Curie–Weiss law. In terms of the theory of Pertsev *et al.* this indicates that the films have undergone a transition to the ferroelectric phase with the polarization vector lying in the plane of the film. Examination of the functional form of the strain dependence of the dielectric properties of a film under this condition shows that the leading terms are identical to those shown in Eq. (2) and that as the dielectric properties measured using a field perpendicular to the polarization axis, changes in polarization in the film introduce only a small correction to Eq. (2).[12] In this letter we therefore proceed by using Eq. (2) to analyze our data and look for deviations from the simple theory for the paraelectric phase that might indicate the presence of in plane polarization.

A combination of Eqs. (1) and (2) gives an expression to correlate experimental data, namely,

$$\frac{1}{c}=\frac{1}{c_i}+t\left(\frac{1}{\varepsilon_u}4Q_{12}\sigma\right), \tag{3}$$

where c_i, ε_u, and Q_{12} are the fitting parameters with the above interpretations. In this letter, we regard the interfacial capacitance c_i and the unstressed film permittivity ε_u as fixed, and focus on the effect of the residual stress on the room temperature dielectric properties.

The films for the study were grown by a chemical vapor deposition process at 700 °C. The constrained sintering may give rise to a stress in the film before cooling, denoted by σ_p. After a temperature drop ΔT, the difference in the thermal expansion coefficients of the film and the substrate, $\Delta\alpha$, gives rise to a strain $\Delta\alpha\Delta T$. When a voltage is applied across the thickness, the film tends to contract in the plane of the film by a strain quadratic in the electric displacement, $Q_{12}D^2$. The constraint of the substrate demands that both the thermal and electrostrictive strains in the film be accommodated by an elastic stress. Consequently, the residual stress in the film is

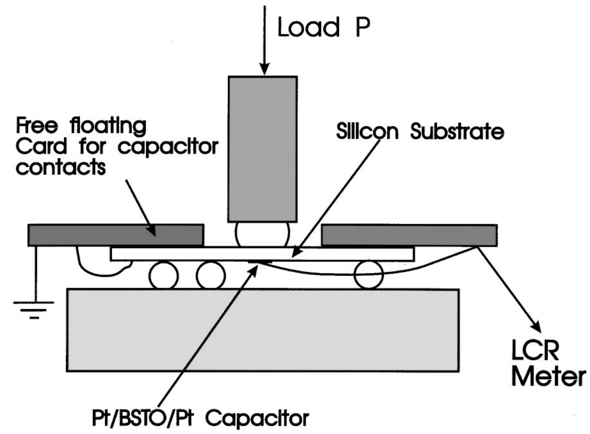

FIG. 2. Experimental setup for measuring capacitance of a BST film under applied load.

$$\sigma=\sigma_p+M_f(\Delta\alpha\Delta T-Q_{12}D^2). \tag{4}$$

Here M_f is the biaxial elastic modulus of the film, and relates to Young's modulus Y_f and Poisson's ratio ν_f by $M_f=Y_f/(1-\nu_f)$. For BST $M_f\approx 200$ GPa. Approximate magnitudes of the various contributions are as follows. The BST film has a larger thermal expansion coefficient than the silicon substrate, $\Delta\alpha\approx 6\times 10^{-6}$/K, so that a temperature drop $\Delta T=680$ K adds to the film a tensile stress of about 800 MPa. The electrostrictive strain $Q_{12}D^2$ is typically below 10^{-3}, giving rise to an additional tensile stress less than 200 MPa. The magnitude of σ_p is affected by the deposition and sintering conditions and is difficult to predict.

We experimentally determined the residual stress in a BST film from the change in curvature on removal of the film from the substrate. A 1×14 cm strip was cut from a wafer. One end of the strip was clamped. Three capacitance gauges were placed on the strip in a line, at a distance $L=4$ cm apart. The displacement reading for every gauge was set to zero when the film was on the strip. The film was then completely etched from the strip using dilute HF, and the new displacement readings were recorded. Let d be the reading from the middle gauge minus the average reading of the two end gauges. The change in the radius of curvature was calculated by $R=2L^2/d$. The residual stress in the film was then calculated by the Stoney equation, $\sigma=Y_sH^2/6tR$, where Y_s is Young's modulus and H the thickness of the substrate.[13] The residual stress level was found to be 610 ± 100 MPa. In a similar experiment the film was progressively removed by ion milling using 0.5 kV argon ions. We found that the average stress in each layer removed was the same, indicating that the residual stress is uniform throughout the film thickness.

To measure the electrostrictive coefficient, we varied the stress in the film by applying a mechanical force. Figure 2

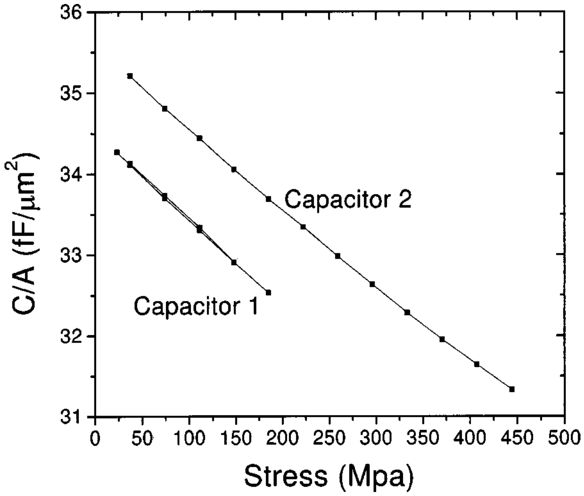

FIG. 3. Measured capacitance per unit film area as a function of the applied stress. For capacitor 1 data on loading and unloading the capacitor are shown. Capacitor 2 was loaded to the fracture of the substrate.

shows our experimental setup. A BST capacitor was made on a Pt coated silicon substrate, which was placed on three ball bearings, and loaded in the center by a punch. The BST capacitor and the punch were on opposite sides of the substrate. Connections to the BST capacitor were made by fine wire contacts silver painted to the Pt top electrode of the capacitor. The wires were bonded to contact pads on a small circuit board placed above the silicon substrate and connected to a Hewlett-Packard 4274A LCR meter. The biaxial stress in the film, induced by the punch load, was calculated from $\sigma_A = K(Y_f/Y_s)(P/H^2)$. Here P is the load applied by the punch, H the thickness of the substrate (730 μm), and K a constant depending on the details of the loading geometry and Poisson's ratio ($K=1.273$ for the test fixtures used).

Figure 3 shows the effect of an applied stress on the capacitance of two capacitors, 1 and 2, prepared on a 96.4 nm thick film. For capacitor 1, the capacitance was measured on increasing and decreasing the load. A superposition of the data indicates that the capacitance change with increasing load is reversible on unloading. For capacitor 2, the data were obtained over a larger range of stress by increasing the load until the substrate fractured. The maximum load applied before fracture was 120 N, corresponding to an increase of 450 MPa in stress in the film.

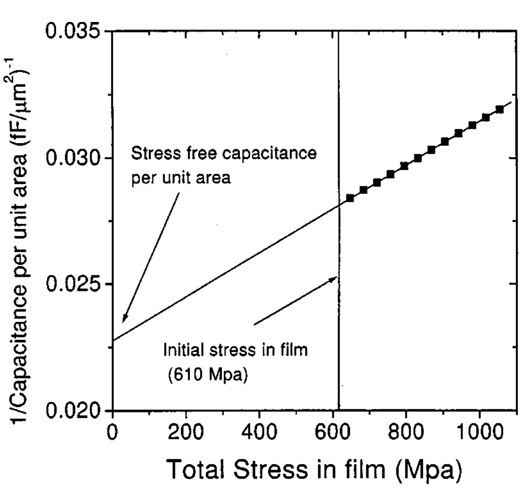

FIG. 4. The relationship between total stress and capacitance and total stress, applied and initial, in a BST film.

Figure 4 plots the data from capacitor 2 in a different way. The vertical axis is the inverse of the capacitance per unit area. The horizontal axis is the sum of the residual stress and the applied stress. The linearity of the plot supports the use of Eq. (3) to interpret the data and indicates that over the stress range examined in the current experiments any correction due to the presence of in-plane polarization is undetectable. From the slope of the plot we estimate the value of the electrostrictive coefficient, $Q_{12}=2.26\times10^{-2}\,\mathrm{m^4/C^2}$. This value is comparable to those of bulk BST. Extrapolating back to zero total stress, we estimate the stress-free specific capacitance to be $44\,\mathrm{fF}/\mu\mathrm{m}^2$, which is about 23% larger than that of the stressed film ($35\,\mathrm{fF}/\mu\mathrm{m}^2$). The possibility that the film undergoes a transformation to a polar phase, as proposed by Pertsev *et al.*[9] cannot be ruled out. However, in the absence of any direct evidence for the formation of polar phases in the film, we believe that present experiments provide a first order assessment of the effect of film stresses on the room temperature capacitance of BST films.

The measurements presented in this letter were conducted on blanket films. The measured film stress at room temperature is comparable to the estimated stress arising from thermal expansion mismatch with the silicon substrate alone. In a dense memory structure the BST film is often deposited onto a three dimensional electrode, and much of the capacitance comes from the BST films on the side walls. In this configuration the thermal expansion mismatch with the electrode structure is likely to be the dominant cause of stress in the film. The currently favored electrode material, platinum, has a thermal expansion coefficient closely matched to that of BST. Consequently, nearly stress free capacitors may be obtained by the appropriate selection of materials. Our results indicate that a 23% increase in capacitance may be obtained by the appropriate mechanical design.

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